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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/733,395	12/12/2003	Hajime Washio	1035-484	9130
23117 7590 08/22/2007 NIXON & VANDERHYE, PC 901 NORTH GLEBE ROAD, 11TH FLOOR ARLINGTON, VA 22203			EXAMINER SHERMAN, STEPHEN G	
			ART UNIT 2629	PAPER NUMBER
			MAIL DATE 08/22/2007	DELIVERY MODE PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

## Office Action Summary

Application No.

10/733,395

Applicant(s)

WASHIO ET AL.

Examiner

Stephen G. Sherman

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 09 July 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-7, 16 and 17 is/are rejected.
- 7) ☒ Claim(s) 8-15 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Continued Examination Under 37 CFR 1.114***

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 9 July 2007 has been entered.

### ***Response to Arguments***

2. Applicant's arguments filed 5 June 2007 have been fully considered but they are not persuasive.

The applicant argued in the response that the section of the specification relied upon by the examiner is not prior art. To prove this, the applicant submitted a Rule 132 Declaration stating that there was a translation error in filing the application, and then following this submission the applicant submitted a certified translation of their Priority Papers. The examiner acknowledges that the Priority Papers confirm that Figures 11 and 12 of the specification were not prior art for their Japanese application, however, the current specification of this application has not been changed to reflect the priority

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papers. Thus the current application still states things such as ""in recent years, the described display device is often used..." and "The present invention is made in view of the FOREGOING CONVENTIONAL PROBLEMS .... ". Accordingly, the examiner maintains the rejection over the current specification, however, the current rejection over the APA will be overcome if the applicant amends the specification to reflect the Priority Papers.

### ***Specification***

3. The disclosure is objected to because of the following informalities:

The specification of the application is not worded the same as the specification of the Priority Papers. Thus the specification should be changed to properly reflect the Priority Papers.

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 1-5, 7 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA (Figures 10-12 and page 2, line 1 to page 8, lines 8.) in view of Kazunari (JP 11-031747).

**Regarding claim 1**, APA discloses a display device (Figure 10), comprising:  
a scanning signal line driving circuit for driving scanning signal lines (Figure 10 shows gate driver GD which drives the gate lines GL(1)-GL(n).); and  
a data signal line driving circuit for driving data signal lines intersecting the scanning signal lines (Figure 10 shows signal driver SD which drives the signal lines SL(1)-SL(n).),

at least one of a scanning signal line driving circuit and a data signal line driving circuit being supplied with at least first and second signals (Figure 11 and page 6, lines 4-18 explain that signals ck1 and ck2 are both supplied to the first data line driver circuit SD1.),

the first signal being supplied in parallel to other circuit than the driving circuit supplied with the first and second signals (Figure 11 shows that the signal ck1 is

supplied also to the second signal driver SD2.), the other circuit being one of the scanning signal line driving circuit, the data signal line driving circuit, and a pre-charging circuit for carrying out pre-charging of the data signal lines (Figure 11 shows that the other circuit is a data driver SD2.),

APA fails to teach the display device further comprising wiring load adjustment section for equalizing wiring load of the second signal which is supplied to the driving circuit, and wiring load of the first signal which is supplied in parallel to the driving circuit and the other circuit.

Kazunari discloses of a display device comprising a wiring load adjustment section for equalizing the wiring load of two signals in which the wirings are of different length (Figure 4 and paragraph [0030] explain that wiring 316 has a partial wiring connected to it, which has a capacitance of 316-A, allowing for the load capacitances of the wirings to be equal.).

Therefore it would have been obvious to “one of ordinary skill” in the art at the time the invention was made to use the teachings of Kazunari with the teachings of APA in order to reduce a difference in delay of the clocks.

***Regarding claim 2***, this claim is rejected under the same rationale as claim 1.

***Regarding claim 3***, please refer to the rejection of claim 1.

**Regarding claim 4**, APA and Kazunari disclose the display device as set forth in claim 2.

APA also discloses wherein the first signal is supplied to the driving circuit and the other circuit from a common input terminal and through a common signal line (Figure 11 shows that the signal ck1 is supplied to the two driving circuits SD1 and SD2 from a common input ck1 and is supplied to both circuits using the same signal line.).

**Regarding claim 5**, APA and Kazunari disclose the display device as set forth in claim 2.

APA also discloses wherein the first and second signals are clock signals of plural systems, respectively (Figure 11 shows that the signals ck1 and ck2 are clock signals.).

**Regarding claim 7**, APA and Kazunari disclose the display device as set forth in claim 2.

Kazunari also discloses wherein the wiring load adjustment section adjusts time constants of the respective wirings of the first and second signals (Figure 4 and paragraph [0030]. The examiner interprets that since the partial wiring is added in order to equalize a delay of the different clock signals, then the time constants are being adjusted.).

**Regarding claim 16**, APA and Kazunari disclose the display device as set forth in claim 2.

APA and Kazunari fail to teach wherein the other circuit is a pre-charging circuit for carrying out pre-charging of the data signal lines, however, it is well known that liquid crystal device can contain a pre-charging circuit for pre-charging the data signal lines.

**Regarding claim 17**, APA and Kazunari disclose the display device as set forth in claim 2.

APA and Kazunari fail to teach wherein the wiring load adjustment section is provided in the scanning signal line driving circuit, however, to place the wiring load adjustment section in a specific location of the circuit would have been a matter of design choice.

7. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over APA (Figures 10-12 and page 2, line 1 to page 8, lines 8.) in view of Kazunari (JP 11-031747) and further in view of Kim (US 5,808,596).

**Regarding claim 6**, APA and Kazunari disclose the display device as set forth in claim 2.

APA and Kazunari fail to teach wherein the signals are digital image signals constituted of a plurality of bits, and are divided into at least two bit groups.



Kim discloses wherein signals are digital image signals constituted of a plurality of bits, and are divided into at least two bit groups (Figure 2 and column 3, lines 40-57 explain that the signals (b) and (c) are pixel data, i.e. image signals, where it is well known that pixel data can be in digital form constituted of a plurality of bits being divided into at least two bit groups.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the idea of compensating for delay of image signals as taught by Kim with the display device taught by the combination of APA and Kazunari in order to create a high resolution liquid crystal display which does not require excessive increases in clock frequency in order to increase resolution.

8. Claims 1-5 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubota et al. (US 2002/0075249) in view of Kazunari (JP 11-031747).

**Regarding claim 1**, Kubota et al. disclose a display device (Figure 26), comprising:

a scanning signal line driving circuit for driving scanning signal lines (Figure 26 shows gate driver GD which drives the gate lines  $GL_j$ - $GL_{j+2}$ ); and

a data signal line driving circuit for driving data signal lines intersecting the scanning signal lines (Figure 22 shows signal driver SD1 which drives the signal lines  $SL_i$ - $SL_{i+3}$ ),

at least one of a scanning signal line driving circuit and a data signal line driving circuit being supplied with at least first and second signals (Figure 26 shows that SD1 is supplied with signals SCK and SCS1.),

the first signal being supplied in parallel to other circuit than the driving circuit supplied with the first and second signals (Figure 26 shows that the signal SCK is supplied also to the second signal driver SD2.), the other circuit being one of the scanning signal line driving circuit, the data signal line driving circuit, and a pre-charging circuit for carrying out pre-charging of the data signal lines (Figure 26 shows that the other circuit is a data driver SD2.),

Kubota et al. fail to teach the display device further comprising wiring load adjustment section for equalizing wiring load of the second signal which is supplied to the driving circuit, and wiring load of the first signal which is supplied in parallel to the driving circuit and the other circuit.

Kazunari discloses of a display device comprising a wiring load adjustment section for equaling the wiring load of two signals in which the wirings are of different length (Figure 4 and paragraph [0030] explain that wiring 316 has a partial wiring connected to it, which has a capacitance of 316-A, allowing for the load capacitances of the wirings to be equal.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the teachings of Kazunari with the teachings of Kubota et al. in order to reduce a difference in delay of the clocks.

**Regarding claim 2**, this claim is rejected under the same rationale as claim 1.

**Regarding claim 3**, please refer to the rejection of claim 1.

**Regarding claim 4**, Kubota et al. and Kazunari disclose the display device as set forth in claim 2.

Kubota et al. also discloses wherein the first signal is supplied to the driving circuit and the other circuit from a common input terminal and through a common signal line (Figure 26 shows that the signal SCK is supplied to the two driving circuits SD1 and SD2 from a common input SCK and is supplied to both circuits using the same signal line.).

**Regarding claim 5**, Kubota et al. and Kazunari disclose the display device as set forth in claim 2.

Kubota et al. also discloses wherein first and second signals are clock signals of plural systems, respectively (Figure 27 shows signals GEN1 and GCK1.).

Therefore it would have been obvious to “one of ordinary skill” in the art at the time the invention was made to use the features of Figure 27 of Kubota et al. with the features of Figure 26 of Kubota et al. and Kazunari in order to reduce a difference in delay of the clocks.

**Regarding claim 7**, APA and Kazunari disclose the display device as set forth in claim 2.

Kazunari also discloses wherein the wiring load adjustment section adjusts time constants of the respective wirings of the first and second signals (Figure 4 and paragraph [0030]. The examiner interprets that since the partial wiring is added in order to equalize a delay of the different clock signals, then the time constants are being adjusted.).

**Regarding claim 16**, Kubota et al. and Kazunari disclose the display device as set forth in claim 2.

Kubota et al. also teach wherein the other circuit is a pre-charging circuit for carrying out pre-charging of the data signal lines (Paragraph [0620]).

**Regarding claim 17**, Kubota et al. and Kazunari disclose the display device as set forth in claim 2.

Kubota et al. and Kazunari fail to teach wherein the wiring load adjustment section is provided in the scanning signal line driving circuit, however, to place the wiring load adjustment section in a specific location of the circuit does not provide any specific benefit and thus would have been a matter of design choice.

9. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kubota et al. (US 2002/0075249) of Kazunari (JP 11-031747) and further in view of Kim (US 5,808,596).

**Regarding claim 6**, Kubota et al. and Kazunari disclose the display device as set forth in claim 2.

Kubota et al. and Kazunari fail to teach wherein the signals are digital image signals constituted of a plurality of bits, and are divided into at least two bit groups.

Kim discloses wherein signals are digital image signals constituted of a plurality of bits, and are divided into at least two bit groups (Figure 2 and column 3, lines 40-57 explain that the signals (b) and (c) are pixel data, i.e. image signals, where it is well known that pixel data can be in digital form constituted of a plurality of bits being divided into at least two bit groups.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the idea of compensating for delay of image signals as taught by Kim with the display device taught by the combination of Kubota et al. and Kazunari in order to create a high resolution liquid crystal display which does not require excessive increases in clock frequency in order to increase resolution.

### **Conclusion**

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10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

16 August 2007

AMR A. AWAD  
SUPERVISORY PATENT EXAMINER  
